



PATENT

#15 / open
TENT 8/26/3
surfer

**THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES**

7 In Re Application of : Vladislav Vashchenko)
8)
9)
10)
11 Serial No.: 09/944,426) Examiner: Ori Nadav
12)
13 Filed: 8/30/2001) Art Unit: 2811
14)
15 For: HIGH HOLDING VOLTAGE
16 LVTSCR-LIKE STRUCTURE)
17)
18)
19)

TECHNOLOGY CENTER 2800

AUG 20 2003

RECEIVED

APPEAL BRIEF
IN SUPPORT OF APPELLANTS' APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

27 Hon. Commissioner of
28 Patents and Trademarks
29 Washington, DC 20231

31 Dear Sir:

32 The Appellants hereby submit this Brief in triplicate in support of their appeal
33 from a final rejection by the Examiner, mailed April 17, 2003 and follow-up Advisory
34 Action mailed August 8, 2003, in the above case. The Appellants respectfully request
35 consideration of this appeal by the Board of Patent Appeals and Interferences for
36 allowance of the above patent application.

37

08/20/2003 RWONDAF1 00000013 09944426

02 FC:1402

320.00 0P

Serial No. 09/944,426

APPEAL BRIEF

37	<u>TABLE OF CONTENTS</u>	
38		
39	I.	REAL PARTY IN INTEREST 4
40	II.	RELATED APPEALS AND INTERFERENCES 4
41	III.	STATUS OF THE CLAIMS 4
42	IV.	STATUS OF AMENDMENTS 5
43	V.	SUMMARY OF INVENTION 5
44	VI.	ISSUES 11
45	VII.	GROUPING OF CLAIMS 11
46	VIII.	ARGUMENT 12
47	IX.	APPENDIX 21
48		20

48 **I. REAL PARTY IN INTEREST**

49 The real party in interest is National Semiconductor Corporation, a corporation of
50 Delaware having a principle place of business at 2900 Semiconductor Drive, M/S D3-
51 579, Santa Clara, CA 95051

52

53 **II. RELATED APPEALS AND INTERFERENCES**

54

55 There are no related appeals or interferences

56

57 **III. STATUS OF THE CLAIMS**

58 Claims 1-6 are currently pending. Claim 1 is withdrawn from consideration and is
59 not being appealed.

60

61 **IV. STATUS OF AMENDMENTS**

62 No after final amendment was made.

63 **V. SUMMARY OF INVENTION**

64

65 The invention relates to a LVTSCR-like structure for electrostatic discharge (ESD)
66 protection, which has a higher holding voltage than a prior art LVTSCR, by including
67 additional p and n regions in a p-well, to define at least one forward biased p-n junction in
68 the p-well.

69 **VI. ISSUES**

70 The issue is whether the prior art cited, namely Ham, discloses a structure having a p-n
71 junction in the p-well that is forward biased during normal operation.

72 **VII. GROUPING OF CLAIMS**

73 Claims 2-6 were rejected based on the common argument that Ham anticipates the
74 invention defined in the claims.

VIII. ARGUMENT

Summary of arguments:

77 Claims 2-6 were rejected under 35 USC 102(b) in view of Ham.

78 The examiner argues that Ham teaches in figure 7 a method that includes
79 providing a p-n junction diode 40,42 in the p-well that is forward biased during normal
80 operation.

It is respectfully submitted that there is no forward biased p-n junction anywhere in Ham. In fact the only biased junctions are the following:

(The regions 40, 42 are both tied to VSS and therefore the p-n junctions across these two regions is not biased. Similarly the regions 50, 52 are both tied to VDD and therefore the junction between them is also not biased.)

94 Thus, Ham has no forward biased junctions.

95 In contrast to Ham, the present application has two p-n junctions in the p-well,
96 namely (p+ region 420/n+ region 422) and (p+ region 424/n+ region 426) (see page 5,
97 lines 36-38). The electric field across the structure between drain 406, 408 and source,
98 biases the two diodes in a forward direction to provide the additional current path when
99 they break down at approximately 1V (see page 6, lines 12-14).

100 The examiner argues that Vdd can be positive or negative and refers to column 4,
101 lines 59-62. There is no such support in the cited section of Ham.

102 The examiner also argues that the limitation of a forward biased p-n junction is
103 not recited in the claims. However the amendment filed February 10, 2003 clearly
104 includes this limitation. In the case of claim 3 it is stated that the current path is from
105 anode to cathode, which is also not disclosed in Ham.

107 Since Claims 2-6 are distinguishable over the prior art, allowance of the claims 2-6 is
108 respectfully requested.

109
110

111

112

113

114

115

116

117

118

119

120

121

122

123

124

125

Charge Our Deposit Account

126

If there are any further charges not accounted for herein, please charge them to our
deposit account No. 140448

128

129

Respectfully submitted,

130

Vollrath & Associates

131

132

133

Date: 5/16/ 2003



134

135

136

137

138

Jurgen K. Vollrath

Reg. No. 49,098

Attorney for Appellants

IX. APPENDIX

2. . A method of increasing the holding voltage of a LVTSCR structure, comprising forming at least one additional p-region and n-region inside a p-well of the structure to define a p-n junction that is forward biased during normal operation.
3. A method of increasing the holding voltage of a LVTSCR-like structure having an anode and a cathode, comprising providing an alternative current path from anode to cathode through a p-well of the structure, other than purely the current path from anode to cathode through the p-material of the p-well.
4. A method of claim 3, wherein the alternative current path defines a lower resistance current path than the p-well.
5. A method of claim 4, wherein the lower resistance current path takes the form of at least one p-n junction that is forward biased under normal operating conditions, formed in the p-well.
6. A method of claim 4, wherein at least one diode is formed in the p-well which provides a low resistance current path once the voltage across the at least one diode is exceeded.